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Fitzpatrick, Cella, Harper & Scinto

SERIAL NUMBER FILING DATE

07/852,740 03/17/92 MORISHITA

FIRST NAMED INVENTOR

M ATTORNEY DOCKET NO.
35-1830

LOKE, S EXAMINER

FITZPATRICK, CELLA, HARPER & SCINTO
277 PARK AVENUE
NEW YORK, NY 10172

ART UNIT PAPER NUMBER
2508

3
02/03/93

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined Responsive to communication filed on _____ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. Notice of References Cited by Examiner, PTO-892.
2. Notice re Patent Drawing, PTO-948.
3. Notice of Art Cited by Applicant, PTO-1449.
4. Notice of Informal Patent Application, Form PTO-152.
5. Information on How to Effect Drawing Changes, PTO-1474.
6.

Part II SUMMARY OF ACTION

1. Claims 1 - 19 are pending in the application.

Of the above, claims _____ are withdrawn from consideration.

2. Claims _____ have been cancelled.

3. Claims _____ are allowed.

4. Claims 1 - 10, 12 - 19 are rejected.

5. Claim 11 is objected to.

6. Claims _____ are subject to restriction or election requirement.

7. This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. Formal drawings are required in response to this Office action.

9. The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are acceptable. not acceptable (see explanation or Notice re Patent Drawing, PTO-948).

10. The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been approved by the examiner. disapproved by the examiner (see explanation).

11. The proposed drawing correction, filed on _____, has been approved. disapproved (see explanation).

12. Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has been received not been received been filed in parent application, serial no. _____; filed on _____

13. Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. Other

FILE NO. 358301

ATTORNEY JSC

DUCE DATE 5/3/93

DOCKETED 2/9/93 mrd

EXAMINER'S ACTION

Serial No. 852,710

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Art Unit 2508

The disclosure is objected to because of the following informalities:

It is believed that the word "gaye" is misspelled in p. 1, line 10. It should be spell as "gate".

There is "200A" in fig. 1. However, there is no "200" in fig. 1. It is believed the word after "of" is "the" in page 12, line 9.

There is no 1006 (page 16, line 1) in fig. 7. It is unclear what is a MOSPET in page 24, lines 21-22.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Appropriate correction is required.

Claims 1-3, 9, 10, 12-14 and 19 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Kawabuchi.

Kawabuchi shows all the elements of the claimed invention in fig. 4 (d). It is a MOSFET comprising: an n type substrate [41] with p+ type source and drain regions [42a, 42b] formed on it; a channel region is formed between the source and drain regions and an insulated gate [44] is formed on it; the channel region comprises a first n type region [46], a second p type region [45] and a third n+ type region [48]; the second p type

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region depleted when the voltage applied to the gate electrode is zero. Kawabuchi further discloses a MOSFET having a first p type region and a second n type region between the source and drain regions in fig. 3.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claim 4 and 15-18 are rejected under 35 U.S.C. § 103 as being unpatentable over Kawabuchi.

Kawabuchi shows the gate oxide [43] has a thickness of 300 Å and the first n type channel region [46] having a thickness approximately equal to the thickness of the gate oxide in fig. 4(d).

Since the mean free path of the drifting carrier has to be 50 to 100 Å or larger, the first channel area of Kawabuchi is larger than the mean free path of the drifting carrier because it

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is approximately equal to 300 Å.

Although Kawabuchi does not show the impurity concentration of the first and second channel region, its specification shows the first and second channel regions having low impurity concentration. Since an impurity concentration of 10^{15} cm^{-3} or below is considered as low impurity concentration, claims 15-16 meet the limitation of Kawabuchi specification.

Although claims 17-18 discloses an n-channel FET, it would have been obvious to one of ordinary skills in the art to have a p-channel FET of Kawabuchi because p-channel FET is complement to n-channel FET.

Claim 5-8 are rejected under 35 U.S.C. § 103 as being unpatentable over Kawabuchi in view of Yazawa et al.

Kawabuchi differs from the claimed invention by not showing the FET is formed on an insulating substrate.

Yazawa et al. shows a MOSFET with reduced short channel effect formed on an insulating substrate in fig. 1B. It comprises: an insulating substrate [8] with n+ source and drain regions [4,5] formed on it; a channel region having a first p region [7] and a second region [6] formed between the source and drain regions [4,5]; an insulated gate [3] formed on the channel region.

Since both Kawabuchi and Yazawa et al. teach a FET with a channel structure to reduce the amount of hot carrier,⁵ it would

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have been obvious to one of ordinary skills in the art to have the insulating substrate of Yazawa et al. in Kawabuchi because it insulates the FET device from other devices.

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication should be directed to Loke at telephone number (703) 308-4920.

Loke/ab
February 01, 1993

W.M.
William Mintel

WILLIAM MINTEL
PRIMARY EXAMINER
GRUJP AU 258

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FITZPATRICK, CELLA, HARPER & SCINTO

TO File	DATE April 23, 1992
FROM Alison Lineen/Andrew Horonick	FILE 35.C8301
SUBJECT	

An inventor search has been done on the above-identified case, and the specification of same has been reviewed for cited references. No items from the inventor search correspond to the product category of the present case. Additionally, no references were cited in the specification of the present case. Consequently, no Information Disclosure materials will be assembled for review at this time.